

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/079,472	02/19/2002	Maitreyee Mahajani	40025-005	6706	
33971	7590 04/20/2005		EXAMINER		
MATRIX SEMICONDUCTOR, INC. 3230 SCOTT BOULEVARD			LE, THAO X		
	RA, CA 95054		ART UNIT PAPER NUMBER		
			2814		
			DATE MAILED: 04/20/2009	s	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)	(2. N)
Office Action Summan		10/079,472	MAHAJANI ET AL.	(Ch)
	Office Action Summary	Examiner	Art Unit	
		Thao X. Le	2814	
Period fo	 The MAILING DATE of this communication Reply 	on appears on the cover sheet w	ith the correspondence address	
THE N - Exten after S - If the - If NO - Failur Any re	PRTENED STATUTORY PERIOD FOR F MAILING DATE OF THIS COMMUNICAT sions of time may be available under the provisions of 37 (siX (6) MONTHS from the mailing date of this communicat period for reply specified above is less than thirty (30) days period for reply is specified above, the maximum statutory to to reply within the set or extended period for reply will, by the ply received by the Office later than three months after the dipatent term adjustment. See 37 CFR 1.704(b).	ION. CFR 1.136(a). In no event, however, may a ion. s, a reply within the statutory minimum of thin period will apply and will expire SIX (6) MON a statute, cause the application to become Al	reply be timely filed ty (30) days will be considered timely. ITHS from the mailing date of this communicat BANDONED (35 U.S.C. § 133).	ion.
Status				
1)⊠	Responsive to communication(s) filed on	19 November 2004.		
2a)⊠	This action is FINAL . 2b)⊠	This action is non-final.		
•	Since this application is in condition for a closed in accordance with the practice ur			is
Disposition	on of Claims			
5) [Claim(s) 9,12-15,24,26 and 36-38 is/are land of the above claim(s) is/are with Claim(s) is/are allowed. Claim(s) 9,12-15,24,26 and 36-38 is/are Claim(s) is/are objected to. Claim(s) are subject to restriction	thdrawn from consideration. rejected.		
Application	on Papers			
9) 🔲 🗆	he specification is objected to by the Exa	aminer.		
10) 🔲 🗆	The drawing(s) filed on is/are: a)	☐ accepted or b)☐ objected to	by the Examiner.	
	Applicant may not request that any objection	- · · · · · · · · · · · · · · · · · · ·		
	Replacement drawing sheet(s) including the of the control of the c	· ·	•	•
Priority u	nder 35 U.S.C. § 119			
12)	Acknowledgment is made of a claim for for All b) Some * c) None of: 1. Certified copies of the priority docu 2. Certified copies of the priority docu 3. Copies of the certified copies of the application from the International E	uments have been received. uments have been received in A e priority documents have been Bureau (PCT Rule 17.2(a)).	Application No received in this National Stage	
Attachment	(s)			
2) Notice Notice 3) Inform	of References Cited (PTO-892) of Draftsperson's Patent Drawing Review (PTO-94) ation Disclosure Statement(s) (PTO-1449 or PTO/5) No(s)/Mail Date	Paper No(Summary (PTO-413) s)/Mail Date nformal Patent Application (PTO-152)	

DETAILED ACTION

Election/Restrictions

1. This application contains claims 3, 5-8, 23, 25, and 40-42 drawn to an invention nonelected with traverse in the amendment filed on 11/19/04. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 102

- 2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
 - (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 9, 12-15, 24, 26, 36-37 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6674138 to Halliyal et al.

Regarding to claims 9, 24 Halliyal discloses a method for making a SONOS device, comprising: providing a channel region 18, column 9 line 1, and providing a first oxide layer 28 on the channel region by ISSG process, column 10 line 33, providing a silicon nitride layer 30, column 1 line 41, on the first oxide layer 28, and providing a second oxide layer 32, column 8 line 63, on the silicon nitride layer 30, wherein the device is a SONOS.

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. The 'N' is silicon nitride in ONO (oxide-nitride-oxide) structure, column 1 line 41. Thus Halliyal either inherently or implicitly discloses nitride layer

Regarding claims 12-15, Halliyal discloses a method wherein the ISSG is performed at a temperature ranging from 700°C to about 1150°C, column 11 line 17, wherein the pressure ranging from 100 torr to about 300 torr, column 11 line 9, wherein the ISSG oxide layer 28 having the thickness of 10 to about 150 angstrom, column 11 line 65, wherein the transistor is a SONOS transistor, wherein the method further including annealing the oxide layer 18 in a nitric oxide atmosphere, column 7 line 39.

Regarding claim 26, Halliyal discloses an integrated circuit containing a SONOS semiconductor device made by the method comprising: providing polysilicon 16, column 10 line 3, providing a first oxide layer 28 on the silicon layer 16 by ISSG, column 10 line 33, providing a silicon nitride layer 30, column 1 line 41, on first oxide layer, and

providing a second oxide layer 32, column 8 line 63, on the silicon nitride layer 30, wherein the device is a SONOS device.

With respect to silicon nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. The 'N' is silicon nitride in ONO (oxide-nitride-oxide) structure, column 1 line 41. Thus Halliyal either inherently or implicitly discloses nitride layer

Regarding claims 36, 37, Halliyal discloses a method for making a SONOS device, comprising: providing a channel region 18, providing a first oxide layer 28 in contact with the channel region by an in-situ steam generation process, column 10 line 33, providing a silicon nitride layer 30, column 1 line 41, in contact with the first oxide layer 28; and providing a second oxide layer 32, column 8 line 63 in contact with the silicon nitride layer 30, fig. 1.

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. The 'N' is silicon nitride in ONO (oxide-nitride-oxide) structure, column 1 line 41. Thus Halliyal either inherently or implicitly discloses nitride layer

Regarding claim 38, Halliyal discloses an integrated circuit containing a SONOS semiconductor device made by a method comprising: providing a silicon wafer or silicon

layer 16, fig. 1, providing a first oxide layer 28 in contact with the silicon wafer or silicon layer 16 by an in-situ steam generation process, column 10 line 33, providing a silicon nitride layer 30, column 1 line 41, in contact with the first oxide layer; and providing a second oxide layer 32 in contact with the silicon nitride layers, fig. 1, wherein the device is a SONOS semiconductor device.

Page 5

With respect to nitride layer 30, Halliyal discloses structure 26 is a modified ONO (28/30/32) structure, column 8 line 27, that can be a combination of various materials including high k material is added to the nitride layer 30 of the conventional ONO, column 12 lines 15-20. The 'N' is silicon nitride in ONO (oxide-nitride-oxide) structure, column 1 line 41. Thus Halliyal either inherently or implicitly discloses nitride layer.

Response to Arguments

4. Applicant's arguments filed on 03 Mar. 2005 have been fully considered but they are not persuasive. The Applicant argues that the layer 30 of Halliyal always includes a high-K dielectric, which cannot be silicon nitride. This is not persuasive because layer 30 of Halliyal is an ONO structure where 'N' is silicon nitride, column 1 line 41. Halliyal attempted to modify the ONO structure by using the high K dielectric material in combination with silicon nitride layer 30 in various embodiments as described in column 12 lines 15-22. Thus, layer 30 would comprise silicon nitride and would read on the claim limitation. It has been held that the use of the term "comprising" leaves a claim open for inclusion of material or steps other than recited in the claims. Ex parte Davis,

80 USPQ 448 (PTO Bd. App. 1948). Use of the term « comprising » does not exclude the presence of the element. In re Hunter, 288 F. 2d 930, 129 USPQ 25 (CCPA 1961).

5. The Applicant argues that claims 3, 5-8, 23, 25, and 40-42 should not have been withdraw from the consideration in the Office Action dated December 09, 2004. The Examiner respectfully submits that the species restriction of those claims were proper as explained in the Office Action dated 11/01/04 and subsequent Office Action dated 12/09/04.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Application/Control Number: 10/079,472 Page 7

Art Unit: 2814

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le 15 April 2005

PRIMARY EXAMINER